WHAT IS CLAIMED IS:

l	1	A method for compiling a design for an integrated circuit, the method
2	comprising:	
3	a	utomatically performing multiple compilations of the design using a series of
4	values for each i	input parameter in a set of input parameters to generate output values for one
5	or more output r	netrics;
5	re	eporting the output values for the output metrics; and
7	C	oncluding the compilations when a stopping criteria has been reached.
1	2	. The method according to claim 1 wherein:
2	tl	he method produces a table of results of the output metrics for each
3	combination of i	input parameters used for a compilation.
1	3	The method according to claim 1 wherein:
2	tl	he method produces a signature of the best configuration of input parameters,
3	for use in future compilations.	
1	4	The method according to claim 1 wherein:
2	tl	he method produces a metric of average results across a range of input
3	parameters to in	dicate expected noise or variability.
1	5	The method according to claim 4 wherein:
2	tl	he metric is used to distinguish gains due to the input parameters from
3	random fluctuat	ion.
1	6	The method according to claim 1 wherein:
2	o	one of the input parameters is a random seed or initial configuration
3	parameter.	
1	7	The method according to claim 1 wherein:
2	o	one of the input parameters is effort level for the compilation tool or a portion
3	of the compilation	on tool.
1	8	The method according to claim 1 wherein:
2	O	one of the input parameters modifies a default cost of a given resource for
3	placement.	

1	9. The method according to claim 1 wherein:	
2	one of the input parameters modifies a default soft-limit for fitting or	
3	synthesis.	
1	10. The method according to claim 1 wherein:	
2	one of the input parameters modifies a coefficient indicating the speed versus	
3	resource usage optimization for the compilations.	
1	11. The method according to claim 1 wherein:	
2	one of the input parameters defines a level of effort to a register packing	
3	algorithm that combines circuit elements in the design into fewer logic elements on the	
4	integrated circuit when enabled.	
1	12. The method according to claim 1 wherein:	
2	one of the input parameters is a balancing parameter to technology mapping in	
3	synthesis.	
1	13. The method according to claim 1 wherein:	
2	one of the input parameters adds or deletes one optimization algorithm or step	
3	from a default CAD flow, or modifies an order in which CAD steps are applied to the	
4	integrated circuit.	
1	14. The method according to claim 1 wherein:	
2	one of the input parameters is a choice or specification of an alternate	
3	synthesis optimization script.	
1	15. The method according to claim 1 wherein:	
2	one of the input parameters enables a netlist optimization or physical	
3	resynthesis step.	
1	16. The method according to claim 1 wherein:	
2	the set of output metrics include a measure of the longest delay path in the	
3	design.	
1	17. The method according to claim 1 wherein:	

2	the	set of output metrics includes a quantification of logic area or other	
3	resource usage of	the integrated circuit.	
1	18.	The method according to claim 1 wherein:	
2	the	set of output metrics includes an estimate of power consumption.	
1	19.	The method according to claim 1 wherein:	
2	the set of output m	netrics includes a metric for a number of paths, register-register pairs, IO-	
3	register pairs, or re	egister-IO pairs that fail to meet a specified timing constraint.	
1	20.	The method according to claim 1 wherein:	
2	the	set of output metrics includes a minimum slack calculated on the	
3	integrated circuit.		
1	21.	The method according to claim 1 wherein:	
2	the	set of output metrics includes a total slack calculated on the integrated	
3	circuit.		
1	22.	The method according to claim 1 wherein:	
2	the	stopping criteria for the method is based on exhausting all possible	
3	combination of spo	ecified input parameters independent of results.	
1	23.	The method according to claim 1 wherein:	
2	the	stopping criteria is based on achieving a user's specified constraints.	
1	24.	The method according to claim 1 wherein:	
2	the	stopping criteria is a total compile time consumed over all of the	
3	compilations thus	far.	
1	25.	The method according to claim 1 wherein:	
2	the	stopping criteria is based on a number of failed constraints in the	
3	integrated circuit.		
1	26.	The method according to claim 1 wherein:	
2	the	stopping criteria for the method is based on the number of failing timing	
3	paths in the circuit.		
1	27.	The method according to claim 1 wherein:	

2	the stopping criteria is based on achieving a minimum worst-case slack in the
3	integrated circuit.
1	28. The method according to claim 1 wherein:
2	the stopping criteria is based on a total slack in the circuit.
1	29. The method according to claim 1 wherein:
2	the stopping criteria is based on a statistical calculation of possible success by
3	the method.
1	30. The method according to claim 1 wherein:
2	an order of configurations tested is a static schedule pre-calculated by a tool.
-	an order of comigatations tested to a state semicate pro-calculated by a took
1	The method according to claim 1 wherein:
2	the order of configurations is dynamically modified based on a metric of
3	current distance from the user goals.
1	32. A computer system for automating compilation of a design for an
2	integrated circuit, the method comprising:
3	code for automatically performing multiple compilations of the design using a
4	series of values for each input parameter in a set of input parameters to generate output values
5	for one or more output metrics;
6	code for reporting the output values of the output metrics; and
7	code for concluding when a stopping criteria has been reached.
1	33. The computer system according to claim 32 wherein the code for
2	reporting the output values further comprises:
3	code for producing a table of results of the output metrics for each
4	combination of input parameters used for a compilation.
1	34. The computer system according to claim 32 further comprising:
2	code for producing a signature of the best configuration of input parameters,
3	for use in future compilations.
1	35. The computer system according to claim 32 further comprising:
2	code for producing a metric of average results across a range of input
3	parameters to indicate expected noise or variability.

1		36. The computer system according to claim 35 wherein the metric is used
2	to distinguish g	gains due to the input parameters from random fluctuation.
1		37. The method according to claim 32 wherein:
2		one of the input parameters is a random seed or initial configuration
3	parameter.	
1		38. The method according to claim 32 wherein:
2		one of the input parameters is effort level for the compilation tool or a portion
3	of the compilat	tion tool.
1		39. The method according to claim 32 wherein:
2		one of the input parameters modifies a default cost of a given resource for
3	placement.	
1		40. A method for determining tuning parameters for a CAD algorithm or
2	tool, the metho	
3		performing multiple compilations of a design of an integrated circuit using a
4		s for each tuning parameter in a set of tuning parameters;
5		performing multiple compilations of the design using a series of exogenous
6	parameters;	
7	-	generating outputs values for one or more output metrics;
8		reporting the output values of the output metrics; and
9		concluding efficacy of the tuning parameters in the presence of exogenous
10	noise.	